## REMARKS

### Summary Of Office Action

Claims 1-53 are pending in this application.

Claims 1, 2, 6, 13-15, 18, 25, 31, 35, 43, 44, and 48 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens et al. U.S. Patent No. 6,226,729 (hereinafter "Stevens") in view of Olarig et al. U.S. Patent No. 6,134,638 (hereinafter "Olarig").

Claims 3-5, 7-12, 16, 17, 19, 20, 26-30, 32-34, 36-39, 41, 45-47, 49, 50, and 51-53 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Olarig, further in view of Johnson et al. U.S. Patent No. 5,577,236 (hereinafter "Johnson").

Claims 21 and 40 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Olarig, further in view of Hartwell U.S. Patent No. 6,724,850 (hereinafter "Hartwell").

Claims 22-24 and 42 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Olarig, and Hartwell further in view of Johnson.

### Summary Of Applicant's Reply

Applicant has proposed amending claims 1-3, 9, 11-13, 25, 26, 29-31. 38, 41, 43-45, and 51-53 to more particularly define the invention.

No new matter would be added by the proposed amendments and all of the amendments are fully justified by the original specification.

Reconsideration of this application in view of the proposed amendments and the following remarks is respectfully requested.

Rejections of Claims
Under 35 U.S.C. § 103(a)

Claims 1-2, 6, 13-15, 18-25, 31, 35, 43, 44, and 48 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens in view of Olarig. Claims 3-5, 7-12, 16, 17, 19, 20, 26-30, 32-34, 36-39, 41, 45-47, 49, 50, and 51-53 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Olarig further in view of Johnson. Claims 21 and 40 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens and Olarig further in view of Hartwell. Claims 22-24 and 24 were rejected under 35 U.S.C. § 103(a) as being obvious from Stevens, Olarig, and Hartwell further in view of Johnson. These rejections are respectfully traversed.

I. Rejections of Independent Claims 1, 13, 25, 31, and 43

Applicant's invention, as defined by proposed amended independent claims 1, 13, 25, 31, and 43 is directed toward a method, computer systems, a memory controller, and an apparatus, respectively, for selecting an operating speed of a memory module interface. The number of memory modules is counted and a running tally of the number of memory modules is maintained based on the counting. Multiple clock signals are generated at different frequencies to provide selectable operating speeds for the memory module interface. One of the operating speeds for the memory module interface is selected based on at least a final tally of the number of memory modules.

Stevens refers to a method for configuring or initializing a memory device. During configuration or initialization, a clock generator is started in the memory controller. The frequency of the a single generated clock signal is selected by "determining a channel frequency at

which all [memory modules] may operate" (Stevens, column 13, lines 43-45).

Olarig refers to a memory controller supporting multiple DRAM circuits that can each operate at a different frequency. Upon initialization, the computer system determines the type of DRAM circuits present and provides status information to the memory controller which, in response, generates multiple clock signals with appropriate frequencies that are respectively applied each DRAM circuit.

The Examiner asserts that the combination of Stevens and Olarig shows all of the elements of applicant's independent claims 1, 13, 25, 31, and 43. Applicant respectfully disagrees with the Examiner's assertion.

In the reply to the previous Office Action, applicant argued that neither Stevens nor Olarig discloses or suggests selecting an operating speed in accordance with the number of memory modules. In response to applicant's argument, the Examiner distinguished between the act of selecting the operating speed based on the counting of the number of memory modules, as was required by applicant's un-amended independent claim 1, and the act of selecting the operation speed based on the number of memory modules. The Examiner asserts that Stevens discloses selecting the operating speed based on the counting of the number of memory modules by "querying the memory modules for various device information to assist in the selection of an operating speed," thereby implying that the querying of Steven is equivalent to "the act of counting" (Office Action, page 22).

Although applicant does not agree with the Examiner's characterization of the act querying as being equivalent to the act of counting, applicant has proposed amending independent claim 1 and 43 to more closely conform to

applicant's independent claims 13, 25, and 31. If amended as proposed, applicant's independent claims 1, 13, 25, 31, and 43 require the operating speed of the memory module interface to by selected from multiple clock frequencies based on at least a final tally of the number of memory modules.

Thus, neither Stevens nor Olarig shows or suggests maintaining a running tally of the number of memory modules and selecting the operating speed of a memory module interface based at least on a final tally of the number of memory modules. Accordingly, whether taken alone or in combination, neither Stevens nor Olarig shows or suggests all of the elements of applicant's amended independent claims 1, 13, 25, 31, and 43.*

Moreover, taken alone neither Stevens nor Olarig discloses or suggests selecting one operating speed for the memory module interface from multiple clock signals generated at different frequencies, and there is no motivation to combine these references in the manner suggested by the Examiner. The Examiner maintains this combination "provides a way to operate memory devices with different operating speeds" (Office Action, page 3, number 9).

Applicant respectfully submits that both Stevens and Olarig independently refer to memory controller systems that may operate memory device with different operating speeds. In

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* The Examiner has criticized applicant's previous reply for attacking the references individually where the rejections are based on a combination. However, any arguments seemingly directed individually at any single reference was intended to demonstrate that the combination of features to which all of references contributed cumulatively fell short of applicant's claimed invention.

fact, Stevens and Olarig disclose contrary techniques for addressing this problem.

Stevens' system "determin[es] a [i.e., one] channel frequency at which all [memory devices] may operate" and generates that one operating speed (Stevens, column 13, lines 43-45).**

In contrast, Olarig's system "generates multiple clock signals with appropriate frequencies for use by the SDRAM memory devices" (Olarig, abstract, lines 3-5).

Thus, Stevens generates a single clock signal of appropriate frequency for all of the memory modules, while Olarig generates a different clock signal for each memory device.

Thus, there is no motivation to combine Stevens and Olarig -- and even if there were -- the combination of Stevens and Olarig still does not result in applicant's invention as defined in independent claims 1, 13, 25, 31, and 43.

Moreover, applicant respectfully submits that the Examiner has employed hindsight reconstruction in combining the references. With the knowledge of applicant's novel system for selecting the operating speed of a memory module interface, particular features of the prior art were identified for use in rejecting applicant's invention. This technique has long been held invalid by the courts at creating a *prima facie* case of obviousness. See In re Fine, 5 USPQ2d

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** The Examiner contends that Stevens discloses applicant's feature of generating multiple clocks at different frequencies by "generating multiple different [clock] speeds in order to determine an appropriate speed" (Office Action, page 22). However, applicant respectfully submits that Stevens does not show generating multiple clock signals at different frequencies. Instead, Stevens refers to generating a single clock signal having a selectable operating speed.

at 1600. ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.").

The Examiner has used applicant's own invention as a bridge between Stevens and Olarig, selecting isolated features of their systems in an attempt show all of the features of applicant's claims. In doing so, the Examiner has demonstrated mere hindsight reconstruction, the very "syndrome" that the requirement for objective evidence is designed to combat, and the rejection is therefore insufficient as a matter of law. See In re Dembiczak, 50 USPQ2d at 1617-1618.

Accordingly, applicant respectfully requests that the rejection of independent claims 1, 13, 25, 31, and 43 be withdrawn.

## II. Rejections of Independent Claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53

The Examiner asserts that the combination of Stevens and Olarig as applied to applicant's independent claims 1, 13, 25, 31, and 43 in further view of Johnson shows all of the elements of applicant's independent claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53. Applicant respectfully disagrees with the Examiner's assertion. In particular, the application of Johnson does not make up for the deficiencies of Stevens and Olarig.

Johnson refers to a memory controller for reading data from synchronous RAM. In Johnson, a sampling clock provides an assortment of sampling clock signals that duplicate the system clock signal with various delays. In response to the number of memory modules present, the clock selector selects one of the delayed sampling clock signals.

Johnson does not disclose or suggest generating multiple clocks at different frequencies. Instead, Johnson discloses generating multiple clocks at the same frequency, but with different amounts of delay.

Thus taken alone or in combination, neither Stevens nor Olarig nor Johnson shows or suggests applicant's claimed feature of generating multiple clock frequencies to provide selectable operating speeds for the memory module interface and selecting a single operating speed for the memory module interface at least partially based on information obtained from memory modules.

Moreover, applicant respectfully submits that the Examiner has employed hindsight reconstruction in combining the references. With the knowledge of applicant's novel system for selecting the operating speed of a memory module interface, particular features of the prior art were identified for use in rejecting applicant's invention. This technique has long been held invalid by the courts at creating a *prima facie* case of obviousness. See In re Fine, 5 USPQ2d at 1600. ("One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.").

The Examiner has used applicant's own invention as a bridge between Stevens, Olarig, and Johnson selecting isolated features of their systems in an attempt show all of the features of applicant's claims. In doing so, the Examiner has demonstrated mere hindsight reconstruction, the very "syndrome" that the requirement for objective evidence is designed to combat, and the rejection is therefore insufficient as a matter of law. See In re Dembiczak, 50 USPQ2d at 1617-1618.

Accordingly, applicant respectfully requests that the rejection of independent claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53 should be withdrawn.

III. Rejections of Independent Claims 21 and 40

The Examiner asserts that the combination of Stevens and Olarig as applied to applicant's independent claims 1, 13, 25, 31, and 43 in further view of Hartwell shows all of the elements of applicant's independent claims 21 and 40. Applicant respectfully disagrees with the Examiner's assertion.

The application of Hartwell for the alleged teaching of the additional elements of claims 21 and 40 does not make up for the deficiencies of Stevens and Olarig. In particular, for at least the reasons discussed above with respect to the patentability of claims 1, 13, 25, 31, and 43, applicant respectfully submits that independent claims 21 and 40 are also not rendered obvious by the combination of Stevens and Olarig in further view of Hartwell.

Accordingly, applicant respectfully requests that the rejection of independent claims 21 and 40 should be withdrawn.

IV. Rejections of Independent Claims 23, 24, and 42

The Examiner asserts that the combination of Stevens and Olarig as applied to applicant's independent claims 1, 13, 25, 31, and 43 in further view of Hartwell and in further view of Johnson shows all of the elements of applicant's independent claims 23, 24, and 42. Applicant respectfully disagrees with the Examiner's assertion.

The application of Hartwell and Johnson for the alleged teaching of the additional elements of claims 23, 24, and 42 does not make up for the deficiencies of Stevens and Olarig. In particular, for at least the reasons discussed above with respect to the patentability of claims 1, 13, 25, 31, and 43, as well as claims 9, 11, 12, 26, 29, 30, 38, 41, and 51-53 applicant respectfully submits that independent claims 23, 24, and 42 are also not rendered obvious by the combination of Stevens and Olarig in further view of Hartwell and Johnson.

V. Rejections of Dependent Claims

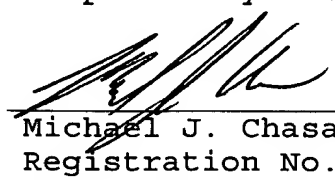
For at least the reasons discussed above with respect to independent claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40-43, and 51-53, dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50, which depend directly or indirectly from claims 1, 9, 11-13, 21, 23-26, 29-31, 38, 40-43, and 51-53 are also not rendered obvious from the combination of Stevens, Olarig, Johnson, and Hartwell (i.e., dependent claims are patentable if their independent claim is patentable).

Accordingly, applicant respectfully requests that the rejections of dependent claims 2-8, 10, 14-20, 22, 27, 28, 32-37, 39, and 44-50 be withdrawn.

Conclusion

The foregoing demonstrates that claims 1-53 are allowable. This application is therefore in condition for allowance. Reconsideration and allowance are accordingly respectfully requested.

Respectfully submitted,



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